Claims

What is claimed is:

1. A processor comprising:

controller circuitry operative to control the storage of a plurality of separate linked list data structures for protocol data units received by the processor;

the linked list data structures being storable in memory circuitry associated with the processor;

wherein the memory circuitry is arranged in a plurality of banks, the plurality of banks being configured to store respective ones of the plurality of separate linked list data structures, such that each of the plurality of banks stores a corresponding one of the plurality of separate linked list data structures; and

wherein the linked list data structures are accessed in an alternating manner that reduces the likelihood of access conflicts between the banks.

2. The processor of claim 1 wherein at least a portion of the memory circuitry associated with the processor comprises an external memory connectable to the processor.

3. The processor of claim 1 wherein at least a portion of the memory circuitry associated with the processor comprises an internal memory of the processor.

4. The processor of claim 1 wherein the memory circuitry comprises a dynamic random access memory (DRAM).

5. The processor of claim 1 wherein the memory circuitry comprises at least four distinct memory banks, each of the four memory banks storing a corresponding one of four separate linked list data structures.

6. The processor of claim 1 wherein the linked list data structures are accessed in an alternating manner by accessing the corresponding memory banks sequentially in accordance with a round-robin selection algorithm.

7. The processor of claim 1 wherein block addresses associated with a given one of the linked list data structures share a common set of lower order bits which identify the corresponding memory bank in which the linked list data structure is stored.

8. The processor of claim 1 wherein a particular linked list data structure to be accessed in a given access interval is determined based at least in part on one or more lower order address bits of block addresses associated with that linked list data structure.

9. The processor of claim 8 wherein the two lowest order address bits are used to identify a particular one of four memory banks to be accessed for a given access interval.

10. The processor of claim 1 wherein the protocol data unit comprises a packet.

11. The processor of claim 1 wherein a given one of the linked list data structures comprises a plurality of entries each having a block descriptor and at least one block address associated therewith.

12. The processor of claim 11 wherein a given one of the block descriptor is associated with a particular data block of a given protocol data unit.

13. The processor of claim 1 wherein the processor is configured to provide an interface for communication of the received protocol data units between a network and a switch fabric.

14. The processor of claim 1 wherein the processor comprises a network processor.

15. The processor of claim 1 wherein the processor is configured as an integrated circuit.

16. A method for use in a processor comprising controller circuitry, the method comprising the steps of:

storing in memory circuitry associated with the processor a plurality of separate linked list data structures for protocol data units received by the processor, wherein the memory circuitry is arranged in a plurality of banks, the plurality of banks being configured to store respective ones of the plurality of separate linked list data structures, such that each of the plurality of banks stores a corresponding one of the plurality of separate linked list data structures; and

accessing the linked list data structures in an alternating manner that reduces the likelihood of access conflicts between the banks.

17. An article of manufacture comprising a machine-readable storage medium having program code stored thereon for use in a processor comprising controller circuitry, the program code when executed in the processor implementing the steps of:

storing in memory circuitry associated with the processor a plurality of separate linked list data structures for protocol data units received by the processor, wherein the memory circuitry is arranged in a plurality of banks, the plurality of banks being configured to store respective ones of the plurality of separate linked list data structures, such that each of the plurality of banks stores a corresponding one of the plurality of separate linked list data structures; and

accessing the linked list data structures in an alternating manner that reduces the likelihood of access conflicts between the banks.